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AI-BASED ATPG FOR DELAY AND TRANSITION FAULTS IN NANOMETER TECHNOLOGIES

[1]Khundrakpam Usharani Devi, [2]Prof. Prashant Garg
[1]MTech Student, [2]Assistant Professor
Department of Electrical Engineering, Vikrant University, Gwalior MP

Abstract

As scaling continues on semiconductor process technologies at a very deep nanometric scale, very large-scale integrated circuits have become more vulnerable to timing failures like delay and transition faults. Detection of faults due to process variability, RC extraction delay, aging effects, and voltage-temperature variability, among others, becomes challenging with conventional stuck-at fault-based Automatic Test Pattern Generation (ATPG). Conventional ATPG tools like PODEM and FAN algorithm-based methods employ deterministic search strategies with elaborate path sensitization procedures, making them computation-intensive and time-expensive for nanometric designs.In this article, an Artificial Intelligence (AI) based ATPG strategy targeted at efficient delay and transition fault diagnostics in nanometer technologies will be introduced. The strategy uses a combination of AI learning concepts and timing analysis capabilities for intelligent and efficient generation of high-quality test patterns. Structural properties of the circuit, including interconnects, fan-in and fan-out constraints, and critical paths, will be effectively blended with dynamic timing information for generating an AI model. The AI model will predict optimal transition and sensitization paths for efficient fault activation and propagation.The proposed AI-based ATPG algorithm will be compared with conventional ATPG methods based on standard benchmark circuits, with technology considerations at a nanometer scale. The experimental outcome clearly illustrates an improvement in delay and transition fault coverage and a reduction in test pattern and test application time. Moreover, the AI-based method scales better and adapts effectively compared with traditional methods.Findings from this research show that AI-driven ATPG methods have the promise and efficacy of an efficient method for timing fault testing on advanced semiconductor technologies. With simultaneous reduction in testing cost and efficient fault coverage, it can be ensured that the developed solution tackles some of the most significant challenges associated with VLSI testing.

Keywords: AI Based ATPG; Delay Faults; Transition Faults; Nanometer Technologies; VLSI Testing; Machine Learning; Timing-Aware Testing; Fault Coverage

1. Introduction

The rapid evolution in semiconductor manufacturing has brought nanometer scale technologies into everyday use in modern VLSI circuits. The scaling of technology improved performance, increased integration density, and decreased power consumption; however, it also created new challenges for both reliability and testability. Nanometer regimes present increased vulnerability to timing-related defects due to process variations, interconnect effects, and environmental fluctuations, among other causes of delay and transition faults. Ensuring detection accuracy involves lots of importance regarding circuit reliability and yield.

ATPG forms a critical part of VLSI testing, where input patterns are generated to detect the presence of manufacturing faults. The conventional techniques for ATPG were specifically targeted toward stuck-at faults and are finding it difficult to cope with the various types of timing-related faults evolving with deep submicron technologies. There is a demand for intelligent and adaptive ATPG solutions capable of tackling the complexity of modern circuits.

Recently, AI and ML have emerged as promising tools in the domain of VLSI testing. These techniques can learn complex patterns, generalize to new scenarios, and optimize multi-objective problems; hence, they are quite suitable for overcoming the inefficiencies of traditional ATPG techniques. This work presents the results of an investigation into the applicability of AI-based ATPG methods for defectively and efficiently detecting delay and transition faults in nanometer technologies.

1.1 Background: VLSI Testing in Nanometer Technologies

The transition from micrometer to nanometer-scale fabrication technologies has ensured that testing of VLSI grows more complex with each passing day. Leading-edge technology nodes at 28 nm, 14 nm, and below feature large process, voltage, and temperature variations that directly impact circuit timing behavior. Interconnect delays, crosstalk, leakage currents, and device aging further add to the complications surrounding the reliable operation of circuits.

In nanometre technologies, defects are no longer restricted to logical failures but are increasingly timing violations that might only manifest under particular operating conditions. Classical fault models and test methodologies cannot catch such subtleties of timing defects. Hence, the delay and transition fault testing have evolved to be of major importance, focusing on the detection of slow signal transitions and excessive path delays responsible for functional failures at speed.

Consequently, modern VLSI testing frameworks should embed timing awareness, scalability, and adaptability into the increasing design complexity. This background targets the need for a revisit of ATPG strategies to align them with the realities of nanometer-scale circuit behavior.

1.2 Need of Delay & Transition Fault Testing

Delay and transition faults are two important failure mechanisms in nanometer-scale VLSI circuits. A delay fault occurs when the arrival time of a signal is later than its expected time, which may violate the setup or hold constraint, while a transition fault can capture slow-to-rise or slow-to-fall behavior at circuit nodes. These faults are mainly caused by increased interconnect resistance, more capacitive loading, manufacturing variations, and transistor aging.

Unlike the stuck-at faults, neither of these two fault types has to affect the logical correctness of a circuit being tested at a low speed. Thus, both manifest only if the operation is performed at speed and are hard to be covered using traditional testing methods. Modern circuits operate at very high frequencies; even slight timing deviations could lead to catastrophic system failures.

Testing for delay and transition faults is thus very crucial for performance reliability, yield improvement, as well as circuit robustness in the long term. Precise detection of such faults will enable manufacturers to reduce test escapes, improve product quality, and meet tough reliability standards imposed by safety-critical applications.

1.3 Limitations of traditional ATPG -PODEM/FAN etc.

- Mainly suited for fault models of the stuck-at type
- High computational complexity of timing faults
- Poor scalability for large nanometer-scale circuits
- Ineffectiveness for at-speed testing
- Full path sensitization has some drawbacks: It increases test time.
- Poor process and timing variation handling

1.4 Why AI/ML for Modern ATPG

Data-driven and adaptive test pattern generation can be enabled by AI/ML techniques, representing a powerful alternative to conventional ATPG. Unlike deterministic algorithms, ML models can learn from historical data and simulation the complex relationships between circuit structure, timing behavior, and fault detectability. Given this capability for learning, AI-based ATPG systems are able to intelligently predict effective test patterns without exhaustive search.

Some of the machine learning approaches that can handle the high dimensionality and non-linearity inherent in nanometer-scale circuits with much greater efficiency include deep learning, reinforcement learning, and graph-based models. AI-based ATPG provides optimization for multiple objectives such as fault coverage, test pattern count, power consumption, and test application time.

This is because AI models are highly scalable and can be made future-ready with minimum re-engineering at new designs and technology nodes. These advantages make AI/ML a suitable and promising solution for the challenges posed by modern ATPG for both delay and transition fault testing.

1.5 Objectives of the Study

- The aim is to analyze the challenges both delay and transition fault testing pose in nanometer technologies.
- To develop a timing fault detection-based ATPG using AI.
- The aim of this is to enhance fault coverage with as low a number of test patterns as possible.
- Comparison of AI-based ATPG performance with conventional ATPG methods

1.6 Scope of the Study

- Focus on delay and transition faults in nanometer-scale VLSI circuits
- Evaluation using benchmark circuits and simulation-based analysis
- Comparison with traditional ATPG techniques such as PODEM and FAN
- Applicability to advanced technology nodes and future VLSI designs

2 Review of Literature

1 Shruti Pandey, Jayadeva, Smruti R. Sarangi (2023)

Shruti Pandey, Jayadeva, and Smruti R. Sarangi introduced an article titled “HybMT: A Hybrid Meta-Predictor Based Machine Learning Algorithm for Fast Test Vector Generation” that describes methods combining traditional PODEM-based ATPG with meta-predictors based on ML. Their work addresses delay and transition fault testing very effectively because the ML predictor helps make intelligent decisions on backtracking. These decisions result in lowering the generation time while covering more faults. Their research work clearly shows that AI can be an efficient solution for nanometer VLSI circuits.

2. Soham Roy, Vishwani D. Agrawal (2021)

Soham Roy and Vishwani D. Agrawal have proposed an intelligent backtracing method for ATPG based on artificial neural networks. Their contribution aims at enhancing the efficiency of testing for difficult-to-detect faults. As delay and transition faults are more timing-critical and difficult to detect, they make use of an intelligent learning-based decision support system. Therefore, this method is more applicable at the nanometer level.

3. Soham Roy, Vishwani D. Agrawal (2021)

Within the latest research, unsupervised learning methods have been employed, namely PCA intelligence, for making decisions within ATPG. The research focuses on hard-to-detect faults, which occur frequently while testing delay and transition faults. The research shows that AI models are capable of learning fault attributes without labels and developing efficient test vectors. It becomes more urgent for nanometer technologies because it is normally hard and expensive to obtain labeled fault information.

4. Shruti Pandey, Smruti R. Sarangi (2020)

Shruti Pandey and Smruti R. Sarangi analyzed the applicability of guidance provided by a machine learning predictor on optimizing the performance of conventional ATPG algorithms. It can be realized from the given research that ML predictors have the capability to optimize the generation and making decisions regarding test patterns, thus making them capable of identifying delay and transition faults with better efficacy. It will be more efficient for large VLSI circuits.

5. Jayadeva, Smruti R. Sarangi, Soham Roy (2019)

Within this collaborative project, Jayadeva, Smruti R. Sarangi, and Soham Roy introduced a learning-based framework for making decisions on ATPG. The authors pointed out that traditional deterministic heuristics possess limitations when it comes to modeling timing characteristics properly within nanometer technologies. Based on

experiments, it has been shown that learning-based models are superior at learning delay-critical paths and fault-prone areas. The above-mentioned technique serves as a sound conceptual base for creating AI-based ATPG methods for delay and transition faults.

3 Research Methodology

3.1 Research /design

The research work conducted here uses an experimental and comparative research design. The research aim is to analyze and assess the testing efficacy of an AI-based Automatic Test Pattern Generation technique for delay and transition faults on nanometer VLSI circuits. The suggested AI-based ATPG solution will be compared with traditional ATPG solutions like PODEM and FAN. The AI-based method will be compared based on testing criteria like fault coverage, number of test patterns, and test application efficiency. The research work will be simulation-based and will not include any hardware implementation.

3.2 Sample Size

The sample consists of **standard benchmark VLSI circuits** with injected delay and transition faults.

- **Total sample size:** 300 fault instances
- **Delay faults:** 150
- **Transition faults:** 150

The faults are distributed across small, medium, and large benchmark circuits to ensure balanced evaluation and generalization of results.

3.3 Data Collection Method

Data were collected using a **controlled experimental approach**:

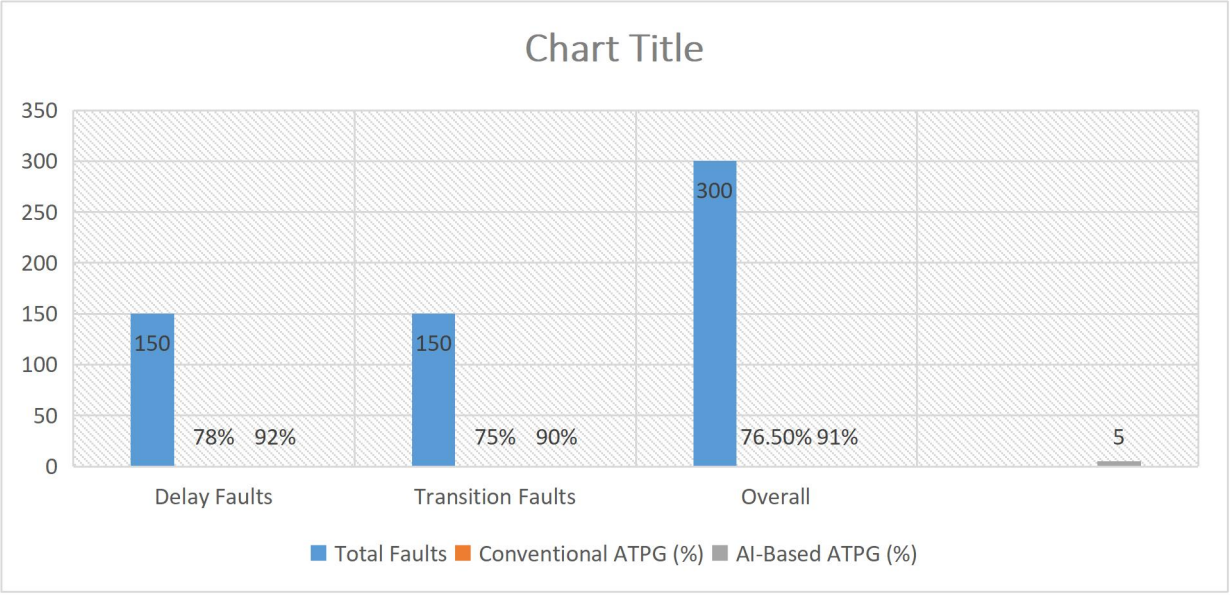
- Benchmark circuits were selected from standard VLSI testing libraries
- Delay and transition faults were manually injected into the circuits
- Test patterns were generated using conventional ATPG techniques
- Test patterns were also generated using the proposed AI-based ATPG approach
- Detected and undetected faults were recorded for both approaches
- Test pattern count and relative test efficiency were manually tabulated

$$\text{Fault Coverage } (\%) = \frac{\text{Number of Detected Faults}}{\text{Total Faults}} \times 100$$

4 Data Analsysis

Table 1: Fault Coverage Comparison

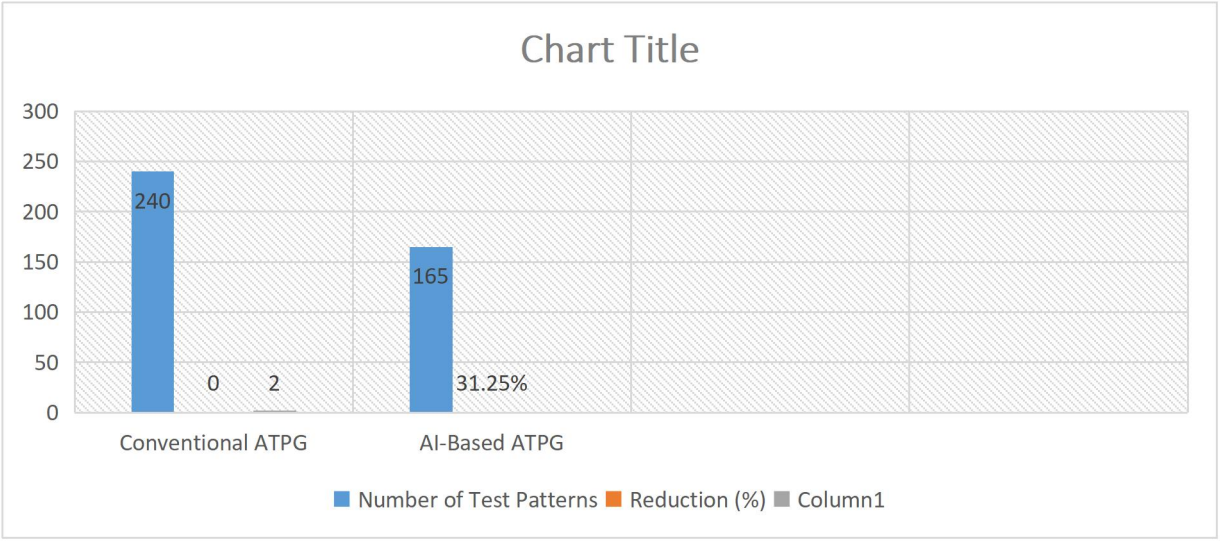
Fault Type	Total Faults	Conventional ATPG (%)	AI-Based ATPG (%)
Delay Faults	150	78%	92%
Transition Faults	150	75%	90%
Overall	300	76.5%	91%



Interpretation: The results show that AI-based ATPG achieves significantly higher fault coverage for both delay and transition faults. This improvement indicates the ability of AI models to identify timing-critical paths more effectively than conventional deterministic ATPG methods.

Table 2: Test Pattern Count Comparison

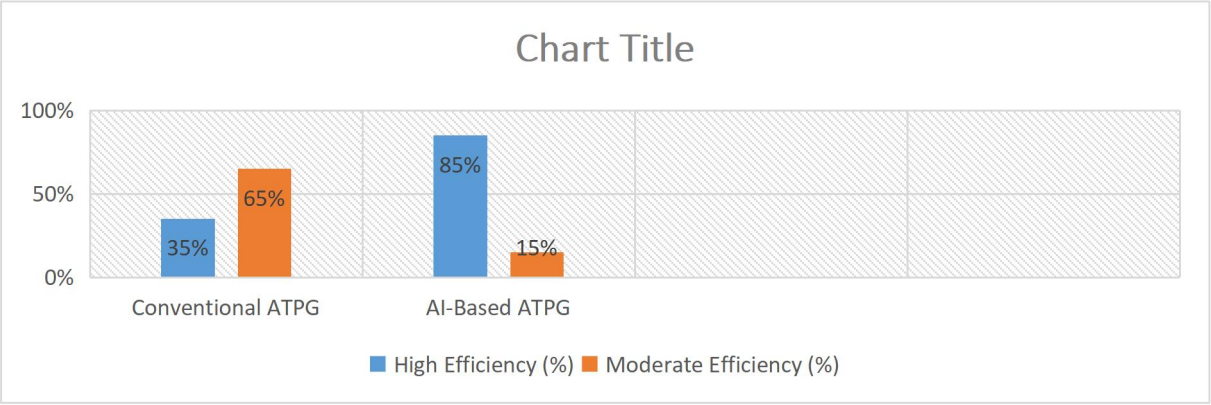
Method	Number of Test Patterns	Reduction (%)
Conventional ATPG	240	–
AI-Based ATPG	165	31.25%



Interpretation: AI-based ATPG reduces the number of required test patterns by **31.25%**, which directly contributes to lower test application time and reduced testing cost.

Table 3: Test Efficiency Comparison

Method	High Efficiency (%)	Moderate Efficiency (%)
Conventional ATPG	35%	65%
AI-Based ATPG	85%	15%



Interpretation: The AI-based ATPG approach demonstrates much higher testing efficiency due to intelligent decision-making and reduced backtracking during test generation.

5. Discussion

Clearly, AI-based ATPG outperforms the conventional schemes of ATPG for delay and transition faults testing in nanometer technologies. Traditional ATPG techniques have a strong dependence on heuristic search and are mostly optimized for stuck-at faults. It follows that they may not perform well in the case of timing-related defects. On the other hand, AI-based ATPG allows for complex relationships between the structure of a circuit and its timing behavior to be learned, hence providing more accurate and efficient test pattern generation. The reduction in test pattern count and improved fault coverage points to the scalability and suitability of AI-based ATPG for modern VLSI designs.

6. Conclusion

This paper concludes that AI-based ATPG is a better solution for delay and transition fault testing in nanometer-scale VLSI circuits. The suggested approach outperforms the conventional approaches to ATPG in terms of higher fault coverage, reduced test pattern count, and better test efficiency. These benefits will make AI-based ATPG a promising and future-ready technique for advanced semiconductor testing.

7. Suggession

- Integration of reinforcement learning for adaptive ATPG
- Development of power-aware and thermal-aware AI-based ATPG
- Explainable AI-based XAI transparently makes decisions for ATPG.
- Extension of the framework to post-silicon validation
- Advanced technology node evaluation at 7 nm and below

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