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LOW-POWER CODED SIGNALING VLSI ARCHITECTURES FOR EDGE-ENABLED IOT SYSTEMS: A REVIEW OF DESIGN TECHNIQUES, INTEGRATION STRATEGIES, AND EMERGING TRENDS

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ABSTRACT

Rapid growth of edge systems that enable Internet of Things (IoT) applications has accelerated the need for power efficient, Very Large-Scale Integration (VLSI) architectures that can handle stringent power, area, and performance constraints. Data transfers between buses, on-chip interconnects, memory interfaces and serial links account for a large portion of energy in edge-IoT devices. This review considers techniques of low power coded signaling, which include bus-invert, shift/rotate-invert, coupling-aware, low-swing, multi-level, serial-link and Network-on-Chip (NoC) coding. It also explores how it connects with near-threshold computing, dynamic voltage scaling, edge-AI accelerators, energy harvesting and edge–fog–cloud architectures. The literature investigated reveals that there is significant potential for energy and power savings, but this will vary with the workload and implementation. Some of the main issues are coding overhead, latency, data dependency, process–voltage–temperature (PVT) variations, signal integrity, reliability, interoperability, and security. Cross-layer energy-aware, data-aware, adaptive and machine-learning assisted VLSI co-design is expected to be the focus of future research.

Keywords: *Low-Power VLSI, Coded Signaling, Internet of Things, Edge Computing, Bus Encoding, Network-on-Chip, Low-Swing Signaling, Edge AI, Energy Efficiency.*

1. INTRODUCTION

The Internet of Things (IoT) is a network of sensing, processing, communication and actuation devices, which are used in applications like healthcare, agriculture, industrial automation, smart home, environment monitoring, transportation, etc. More and more data is being created and manipulated at the network edge, where devices have limited thermal dissipation, small form factor and battery size [1]. Hence, the design of energy efficient VLSI for reliable operation of edge-IoT is crucial. Dynamic power is significant in advanced CMOS systems because switching activity in buses, on-chip interconnects, memory interfaces and serial links are all significant components. When interconnect width, frequency and length grow, wire capacitance is an important cause of energy consumption. To cure this problem, coded signaling is used to convert transmitted data so that it causes fewer signal changes or voltage swings.

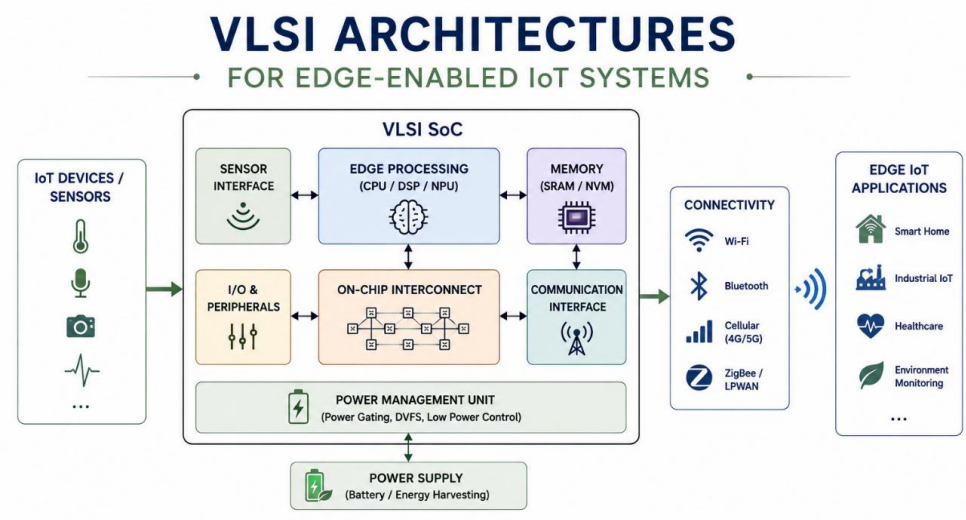

Figure 1: VLSI Architecture for Edge Enabled IoT Systems [2]

The dynamic power of a CMOS circuit can be approximated as:

$$P_{dynamic}=\alpha C_L V_{DD}^2 f$$

where α represents switching activity, C_L is effective load capacitance, V_{DD} is supply voltage, and f is operating frequency. Thus, reducing switching activity and supply voltage can substantially lower dynamic power.

For edge-IoT architectures, coded signaling is an excellent option. Bus-invert and coupling-aware coding limit switching activity and low-swing and current-mode signaling limit voltage excursions. Multi-level signaling leads to more information sent per symbol. These methods can work in addition to clock gating, power gating, DvS, and NTO [3].

With growing adoption of edge AI, the need for energy-efficient data transfers becomes more crucial as accelerators are constantly moving activations, weights, and intermediate results. Likewise, when using limited or intermittent power energy harvesting devices can gain from lower energy required for communication. This review hence discusses the study of low power coded signaling from circuit and architectural point of view with emphasis on their application to VLSI architectures for edge enabled IoT systems.

1.1. Objectives of the Review

The objectives of this review are:

- To examine major low-power coded signaling techniques for reducing switching activity and dynamic power in VLSI interconnects used in IoT edge nodes.
- To analyze the integration of coded signaling with near-threshold computing, edge-AI accelerators, and energy-harvesting technologies.
- To identify the key benefits, challenges, and emerging research directions for energy-efficient coded signaling VLSI architectures.

2. REVIEW METHODOLOGY

In this study, an integrative literature review methodology is used, where the topic of interest is Low power VLSI, coded signaling, bus and NoC encoding, near threshold computing and edge-IoT architectures [4]. Google Scholar, IEEE Xplore, SpringerLink, Science Direct, MDPI and arXiv were used to identify relevant literature.

Studies published in the period 2019-2026 were given priority, and some earlier studies were selected to provide the basic concepts. The literature was divided into five themes: (1) coded-signaling fundamentals, (2) bus, NoC, and serial-link techniques, (3) integration with near-threshold, edge-AI, and energy-harvesting systems, (4) benefits and challenges, and (5) emerging trends. Power, energy, and switching-activity results for studies with direct relevance to resource-constrained IoT VLSI were highlighted. Theoretical coding studies without results from implementation and simulation and studies of IoT without any VLSI content were excluded. This is not a statistical meta-analysis, but a qualitative and descriptive review.

3. CONCEPTUAL FRAMEWORK OF LOW-POWER CODED SIGNALING

The conceptual framework provides an explanation on how coded signaling minimizes switching, voltage transition, and energy consumption in VLSI interconnects in edge-enabled IoT systems.

3.1. Coded Signaling in VLSI Interconnects

In CMOS circuits, the switching of signals results in charging and discharging of capacitances. Hamming Distance can be used to represent the number of transitions between consecutive data words [5]:

$$HD(D_i,D_{i-1})=\sum_{k=1}^{n}(D_{i,k}\oplus D_{i-1,k})$$

where D_i and D_{i-1} are consecutive data words and n is the bus width. Coded signaling minimizes such a number of

transitions without compromising the information being sent. A basic coded-signaling architecture consists of an encoder, communication channel, and decoder.

3.2. Bus-Invert Coding

Bus-invert coding compares adjacent data words and sends the original or the complement of the data word, whichever results in fewer transitions. This is a simple method and is the foundation of many more sophisticated coding methods. Some area and power overhead, however, for other control and codec logic [6].

3.3. Coupling-Aware Signaling

Coupling-aware coding takes into account switching activity as well as switching of individual bits between adjacent wires. It can minimize power dissipation and crosstalk in the interconnects due to the reduction in high coupling switching patterns. The effectiveness is related to the structure and complexity of the bus.

3.4. Low-Swing and Multi-Level Signaling

Low-swing signaling results in lower voltage swings of transmitted signals, which in turn results in lower energy per transition [7]. Multiple-level signaling and Pulse-Amplitude Modulation (PAM) use multiple levels of voltage or current to represent more information with each symbol. These techniques can lead to energy savings, but they have lower voltage margins, meaning they are more vulnerable to noise, process variations, and signal-integrity issues.

4. MAJOR CODED SIGNALING TECHNIQUES FOR LOW-POWER IOT VLSI

Low-power coding methods can be simply categorized as those that reduce the number of bit transitions, coupling activity, voltage swing or the number of symbols transmitted.

Table 1: Major Coded Signaling Techniques for Low-Power VLSI Interconnects [8]

Technique	Main Principle	Major Advantage	Main Limitation
Bus-Invert Coding	Transmit original or complemented word	Simple transition reduction	Additional flag and logic
Shift/Rotate-Invert Coding	Select shifted, rotated, or inverted data	Greater transition reduction	Higher complexity
Coupling-Aware Coding	Minimize self and adjacent-wire switching	Reduces coupling power	Requires more encoding logic
Low-Swing Signaling	Reduce signal voltage excursion	Lower dynamic energy	Reduced noise margin
Current-Mode Signaling	Use controlled current transmission	Low swing and high speed	Receiver complexity
Ternary/PAM Signaling	Use multiple signal levels	More information per transition	Signal-integrity problems
Serial Correlation Coding	Exploit temporal data correlation	Lower serial switching	Data dependent
NoC Link Coding	Encode transmitted flits/packets	Lower NoC power	Codec latency
Error-Correcting Codes	Combine low-power coding with error protection	Energy and reliability benefits	Redundancy overhead
Adaptive Coding	Change coding based on data statistics	Workload-specific savings	Control complexity

It is known from the literature that when the implementation complexity of bus-invert and its derivatives is relatively low, they continue to be attractive. Further more sophisticated methods have been developed that incorporate the coupling of activity, the physical signal swing, and the data correlation in the optimization objective.

- **Shift- and Rotate-Invert Coding:** These techniques choose between alternative representations of data that are shifted, rotated or inverted to minimize the number of transitions. These can offer a more significant saving over simple bus-invert encoding, but need extra selection logic [9].
- **Shift- and Rotate-Invert Coding:** The idea of serial coding is to take advantage of the correlation between adjacent data symbols to minimize switching activity. The reported reductions are up to 48.8% for certain data patterns.
- **NoC Coding:** NoC coding decreases switching/coupling activity in on-chip communication. Power savings reported range from 30% to over 60% depending on traffic and architecture, depending on the approach.
- **Error Correcting Low Power Codes:** These are the techniques that use both energy efficient signaling and error protection. They provide increased reliability, but consume more hardware overhead as more redundancy and decoding circuits are added.

5. INTEGRATION WITH EDGE-IOT TECHNOLOGIES

The best opportunity of coded signaling is a combination with other low power technologies. Coding can be used to complement voltage scaling or power management, rather than replacing them.

5.1. Near-Threshold and Sub-Threshold Computing

Near-threshold operation is achieved by lowering the supply voltage to a voltage near the transistor threshold [10]. This can offer great energy savings, however may also make this process more sensitive to variation in the process, temperature, uncertainty in timing and noisier. Coded signaling can be used in conjunction with near-threshold operation to decrease the number of transitions, and voltage scaling can be used to decrease the energy associated with each transition. Thus,

$$E_{link} \propto N_{transitions} C V_{DD}^2$$

where $N_{transitions}$ is the number of signal transitions.

The two combinations can then result in even more energy savings than either method on its own. A study of 55-nm microcontrollers found a 27.98% energy reduction with deep path activity detection and dynamic voltage scaling using an operating point that was determined to be minimum energy.

5.2. Edge-AI Accelerators

Edge AI increases the amount of data processed locally. Neural-network accelerators transfer the activation, weights, partial sums and intermediate feature maps between memories and processing elements. Energy of the communication process can thus be a significant component of accelerator power. Coded signaling can be used for internal bus and NoC links to minimize unnecessary switching [11]. Other opportunities may arise from the fact that the activity in such architectures is usually sparse, like neuromorphic and event-driven ones. The literature reviewed covers architectures with significant power savings with respect to traditional solutions, such as approximately 5-fold power savings reported for certain neuromorphic edge-AI implementations.

5.3. Energy-Harvesting IoT

Energy harvesting is the process of obtaining energy from various sources including solar radiation, radio-frequency energy, vibration energy and thermal gradient. These are intermittent and the available energy levels may fluctuate significantly. The duty cycle of an energy-harvesting node can be raised by lowering the communication energy used for coded signaling. Coding can be used in conjunction with adaptive duty cycling, power gating and energy aware task scheduling.

5.4. Edge–Fog–Cloud Architectures

Edge–fog–cloud architectures spread out computation over a number of tiers. Thus, the edge device is not enough to ensure energy efficiency; communication and task allocation in the hierarchy are also important factors.

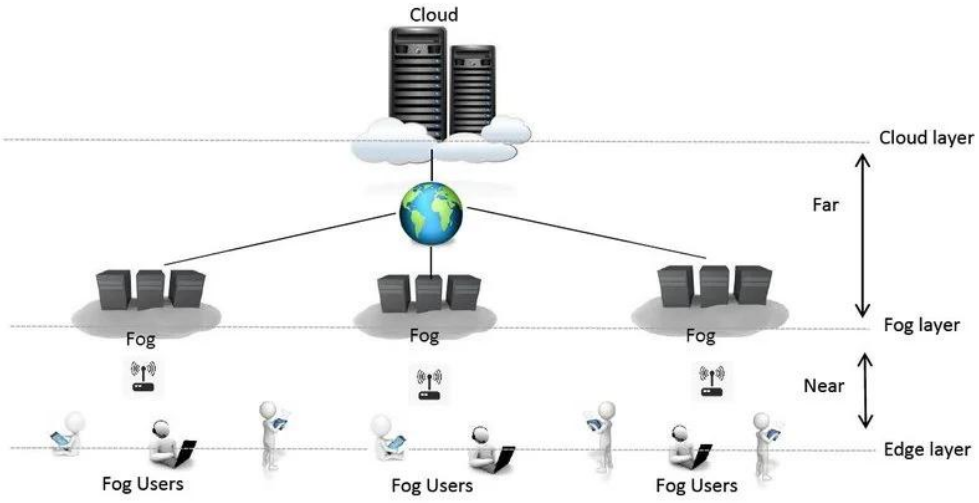

Figure 2: Edge–Fog–Cloud Architectures [12]

Energy used for data movement between edge, fog and cloud resources can be reduced by using node-selection and offloading strategies. In addition to these strategies, coded signaling at the device level can be used to reduce energy used in the local communication paths within the VLSI.

Table 2: Integration of Coded Signaling with Emerging Edge-IoT Technologies

Study/Approach	Integration Area	Main Contribution
Peltekis et al. (2023) [13]	Bus coding + clock gating	Combines bus-invert coding with zero-value clock gating
Yu et al. (2023) [14]	Near-threshold VLSI	DVS with deep path activity detection; 46.95% reported energy reduction
Vaibhav (2025) [15]	Neuromorphic edge AI	Low-power spike-based architecture with reported five-fold power reduction
Badami et al. (2026) [16]	Edge-AI VLSI	Approximate computing and dataflow acceleration; up to 42% reported power saving
Rahim (2025) [17]	Edge–fog–cloud	Energy-aware node selection across layered IoT architecture

The works summarized above illustrate the evolution in the design space from a circuit level optimization to a cross-layer design that incorporates coding, voltage scaling, computation and communication.

6. BENEFITS OF LOW-POWER CODED SIGNALING

Compared to the traditional approach, low-power coded signaling has a number of benefits in terms of energy savings and efficient communication in an edge-enabled IoT system where hardware resources are limited [18]. The main advantages are: lower dynamic power, longer battery life, better thermal performance, better signal integrity, compatibility with existing low-power methods, scalability throughout various VLSI communication architectures.

a) **Dynamic Power:** Coded signaling is used to minimise unnecessary switching of signals, which reduces the charging and discharging of interconnect capacitance and therefore reduces dynamic power consumption [19].
b) **Extended Battery Life:** Minimized communication energy allows battery-powered IoT sensors to have longer battery life, especially in locations with limited reach or access.
c) **Enhanced Thermal Performance:** By operating with reduced switching activity, peak current and heat are also minimized, ensuring consistent performance in a wide range of IoT applications that have limited thermal dissipation.

d) **Enhanced Signal Integrity:** Coding that is considered for coupling can limit unwanted interactions between adjacent wires, which can help minimize crosstalk and timing variations.
e) **Compatibility and Scalability:** Coded signaling can be used alongside other techniques including clock gating, power gating, dynamic voltage/frequency scaling and near threshold operation [20]. It can also be used in buses, NoCs, serial connections, memory interfaces, and other interconnects to enable heterogeneous IoT SoCs.

7. CHALLENGES AND DESIGN TRADE-OFFS

While coded signaling can markedly decrease interconnect energy, it has certain design constraints that limit its effectiveness in practice [21]. Additional energy benefit can be lost due to the area, power, and latency of the encoder and decoder circuits. The performance of the coding also depends on the nature of the data being transmitted, for some types of coding, random or burst traffic is not suited. Moreover, the low swing, multi-level and near threshold signaling are sensitive to process, voltage and temperature (PVT) variations and offers lower noise margins and demands careful circuit and physical design.

Other issues involved are complexity of hardware, interoperability, reliability and security. In complex coding schemes, additional multiplexers, comparators, control logic, and memory are needed, which increases the area and implementation complexity of the resource scarce IoT devices [22]. This also makes it challenging to integrate and compare the performance of the coding approaches across platforms. Error correcting techniques increase reliability but also create redundancy and processing overhead, and coded data must be compatible with both the encryption and authentication systems. Hence, there is a need for a compromise between energy saving, space, latency, reliability and security for low power coded signaling.

8. EMERGING TRENDS AND FUTURE RESEARCH DIRECTIONS

The next generation of low-power coded signaling is looking towards adaptive and data-aware coding, where the coding method can be chosen based on the workload and characteristics of the data, as they are received [23]. The optimization of coding for supply voltage, frequency and switching activity of the processors is also interesting, especially for near-threshold processors on the edges. Coded signaling is also being investigated to enable edge-AI dataflows, where activation streams and weight streams can be intertwined, and sparse computation and zero-value gating can be implemented to minimize data-movement energy [24].

Another critical one is energy harvesting-enabled and machine learning-driven coding, where coding complexity can be adjusted to the energy available, and also optimization of coding, voltage scaling, clock gating and physical implementation can be done using a machine learning tool. Security conscious coding is becoming more significant, and it requires efficient coordination of coding, error detection/decoding, encryption and authentication [25]. Overall, the future systems will be adaptive, cross-layer co-design systems instead of fixed and isolated coding techniques.

9. CONCLUSION

The low-power coded signaling method is an effective solution for the reduction of energy consumption in the communication paths of VLSI embedded in edge-enabled IoT systems. This review demonstrates that techniques like bus-invert, shift/rotate-invert, coupling-aware coding, low swing and multi-level signaling, serial-link coding, and NoC link encoding can lower switching activity, voltage transitions and communication-related dynamic power. The integration of near-threshold computing, dynamic voltage scaling, edge-AI accelerators, energy harvesting, and edge–fog–cloud architectures further illustrate the ability of coded signaling to be a complementary aspect of a cross-layer energy-efficient design. Yet, adoption is held back by encoder/decoder overhead, latency, data dependence, PVT variation, lower noise margins, signal integrity, reliability, interoperability and security. Based on this, it is concluded from the reviewed literature that the future VLSI architectures should be based on adaptive, data-aware and energy-aware strategies and architectures that can optimally manage communication, computation and power management. Overall, low-power coded signaling is a promising design approach for building scalable, reliable, and energy-efficient VLSI architectures to meet the increasing demands of the next generation of edge-IoT systems.

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